CLAIMS

What is claimed is:

1. Circuitry in a field-programmable gate array (FPGA) including an array of random access memory cells comprising at least one row of a plurality of random access memory cells, each of said plurality of random access memory cells is coupled to a row driver line, said circuitry comprising:

a row decoder coupled to a first end of said row driver line; and

a monitoring memory cell coupled to said row driver line and a memory writing line.

2. The circuitry of Claim 1 wherein said monitoring memory cell is coupled to a second end of said row driver line.

3. The circuitry of Claim 1 wherein said monitoring memory cell is coupled to said row driver line at each corner of said array of RAM memory cells.

4. A method for clearing each of a plurality of random access memory cells in an array of random access memory cells in a filed programmable gated array acting as the programming mechanism, wherein said field programmable gated array further having erase circuitry for clearing said array of said random access memory cells for reprogramming of said field programmable gated array and a monitoring memory cell coupled to said erase circuitry and said array of random access memory cells, said method comprising:

initiating a memory clear phase on said at least one monitoring memory cell;

reading said monitoring memory cell responsive to said memory clear phase; and

determining whether the output signal from said monitoring memory cell indicates a cleared monitoring memory cell.

5. The method of Claim 4, further comprising:

performing said memory clear phase a second time responsive to a determination that the output signal from said monitoring memory cell indicates that said monitoring memory cell is not cleared.

6. The method of Claim 5, further comprising:

counting a number of times that said memory clear phase is performed;

determining whether said number of times is equal to a threshold; and

generating an alarm responsive to said number of times being greater than said threshold.

7. A method for performing a write function in an array of random access memory cells in a field programmable gated array of a plurality of random access memory cells as a programming mechanism wherein said field programmable gate array includes write circuitry for verifying a write operation that is connected to a monitoring memory cell, the method comprising:

performing said write operation;

reading said monitoring memory cell; and

determining whether the output signal from each said at least one monitoring memory cell indicates a proper write operation performed on said monitoring memory cell.

8. The method of Claim 7, further comprising:

performing said memory write a subsequent time responsive to a determination that the output signal from said monitoring memory cell indicates that said monitoring memory cell was not properly written to.

9. The method of Claim 8, further comprising:

counting a number of times said memory write is performed;

determining whether said number is at least equal to a threshold; and

generating an alarm if the method returns to said memory write phase more than a predetermined number of times.

10. An apparatus in a field programmable gate array capable of verifying the functioning of an array of a plurality of random memory cells in said filed programmable gate array wherein said filed programmable gate array includes erase circuitry and a monitoring memory cell connected to said erase circuitry, comprising:

means for initiating a memory clear phase on said at least one monitoring memory cell; and

means for determining whether the output signal from each said at least one monitoring memory cell indicates a cleared monitoring memory cell.

11. The apparatus of Claim 10, further comprising:

means for performing said memory clear phase a subsequent time responsive to a determination that the output signal from said monitoring memory cell indicates said monitoring memory cell is not cleared.

12. The apparatus of Claim 11, further comprising:

means for counting a number of times said memory clear phase is performed;

means for determining whether said number of times is greater than a threshold; and

means for generating an alarm responsive to said counter is greater than said threshold.

13. An apparatus in a field programmable gated array capable of verifying the functioning of an array of a plurality of random access memory cells in said field programmable gate array, wherein said filed programmable gate array includes write circuitry for writing data in said array of said plurality of random access memory cells and a monitoring memory cell coupled to said write circuitry, said apparatus comprising:

means for performing a memory write phase on said monitoring memory cell; and

means for determining whether an output signal from said monitoring memory cell indicates a properly memory written to monitoring memory cell.

14. The apparatus of Claim 13, further comprising:

means for performing said memory write phase a subsequent time responsive to a determination that the output signal from at least one monitoring memory cell indicates that said monitoring memory cell was not properly written to.

15. The apparatus of Claim 14, further comprising:

means for counting a number of times said memory write phase is performed;

means for determining whether said number of times is greater than a threshold; and

means for generating an alarm responsive to a determination to said memory write phase more than a predetermined number of times.